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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,890	01/30/2004	Yasurou Matsuzaki	100353-00181	4185

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EXAMINER	
TRAN, LONG K	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,890	MATSUZAKI, YASUROU	
	Examiner	Art Unit	
	Long K. Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004 and 14 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 -12, 16-25, 29-41* is/are pending in the application.

4a) Of the above claim(s) *1-12,16,17,22-25,29 and 31-41* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-21 and 30* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/956,973.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/30/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is in response to Amendment filed on January 30, 2004.

2. Claims **13 – 15** and **26 – 28** have been cancelled.

3. Claims **16** and **17** have been amended.

Election/Restrictions

4. Applicant's election without traverse of claims **13 – 21** and **30** in the reply filed on September 14, 2004 is acknowledged.

5. Claims **1 – 12, 16, 17, 22 – 25, 29** and **31 – 41** withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected claim, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on September 14, 2004.

6. Claims **18 – 21** and **30** are presented for examination.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/956,973, filed on September 21, 2001.

Information Disclosure Statement

7. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on January 30, 2004.

Information disclosed and lists on PTO 1449 were considered.

Claims Objection

8. Claim **20**, the examiner is unable to find "a third wiring layer", " second semiconductor substrate" and "a fourth wiring layer" in the specification. Clarification is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims **18 – 15** are rejected under 35 U.S.C. 102(e) as being anticipated by Suyama (US Patent No. 6,403,463).

Regarding claim **18**, figures 1 – 3 illustrate a multi-chip semiconductor apparatus in which a first chip and a second chip coexist and each of the first and second chips includes circuit components, one of the first and second chips comprising:

a first wiring layer 56 provided on a semiconductor substrate 1;

a second wiring layer 57 provided on an insulating layer 52 covering the first wiring layer, the second wiring layer including conductive lines (with terminal 2b and 2c) each interconnecting the circuit components of said one of the first and second chips;

a first electrode 56 (with terminal 2a) provided in the first wiring layer 56 (col. 2, lines 57 – 58); and

a plurality of first electrodes (with terminals 2a) provided in the first wiring layer, and a second electrode (with terminals 2b and 2c) provided on each of the conductive lines, each conductive line being configured to interconnect the plurality of first electrodes and the second electrode;

Wherein the plurality of second electrodes are provided such that, when the first and second chips are combined together, the plurality of second electrodes contact corresponding electrodes of other of the first and second chips so that the conductive lines interconnect the first and the second chip via the plurality of second electrodes 57 (col. 3, lines 3 – 12).

Regarding claim **19**, figures 1 – 3 illustrate a multi-chip semiconductor apparatus in which a first chip and a second chip coexist and each of the first and second chips includes circuit components, one of the first and second chips comprising:

a first wiring layer 56 provided on a semiconductor substrate 1;

a second wiring layer 57 provided on an insulating layer 52 covering the first wiring layer, the second wiring layer including conductive lines (with terminals 2c and 2b) each interconnecting the circuit components of said one of the first and second chips;

a plurality of first electrodes 56 (with terminals 2a) provided in the first wiring layer 56, and

a plurality of second electrode 57 (with terminals 2b and 2c) provided on each of the conductive lines, each conductive line being configured to interconnect the plurality of first electrodes and the second electrode.

Regarding claim **20**, figures 1 – 3 illustrate a multi-chip semiconductor apparatus in which a first chip and a second chip coexist and each of the first and second chips includes circuit components, the first comprising:

a first wiring layer 56 provided on a semiconductor substrate 1;

a second wiring layer 57 provided on a first insulating layer 52, the first wiring layer, the second wiring layer including conductive lines each interconnecting the circuit components of said one of the first and second chips;

a first electrode provided in the first wiring layer 56 (col. 2, lines 57 – 58); and

a second electrode (with terminals 2b and 2c) provided on each of the first conductive lines (fig. 2), each conductive line being configured to interconnect the first electrode and the second electrode;

the second chip (LSI chip; noted: Suyama does not show separate chips as firs and second. However, Suyama does show all four LSI chips with identical structures as shown in figures 1 – 3) comprising:

a third wiring layer 56 provided on a second semiconductor substrate 1;

a fourth wiring layer 57 provided on a first insulating layer 52, the first wiring layer, the second wiring layer including conductive lines each interconnecting the circuit components of said one of the first and second chips;

a third electrode 56 (with terminals 2a) provided in the third wiring layer 56 (col. 2, lines 57 – 58); and

a fourth electrode 57 (with terminals 2b and 2c) provided on each of the second conductive lines (fig. 2), the fourth electrode being arranged such that, when the first

and second chips are combined together, the fourth electrode contacts the second electrode (noted: because the LSI chip having identical structure, therefore, second electrode 57 (with terminals 2b and 2c) of the first chip is same as the fourth electrode 57 (with terminals 2b and 2c) of the second chip; figure 3 illustrates wiring in wiring 57 is shared between two LSI chip; and the two electrodes will contact each other when the chips are combined together).

Regarding claim **21**, figures 1 – 3 illustrate a multi-chip semiconductor apparatus in which a first chip and a second chip coexist and each of the first and second chips includes circuit components, the first chip comprising:

a first wiring layer 56 provided on a semiconductor substrate 1;

a second wiring layer 57 provided on a first insulating layer 52 covering the first wiring layer, the second wiring layer including conductive lines each interconnecting the circuit components of said one of the first chip;

a first electrode 56 (with terminal 2a) provided in the first wiring layer 56 (col. 2, lines 57 – 58); and

a second electrode (with terminals 2b and 2c) provided on each of the first conductive lines (fig. 2), each conductive line being configured to interconnect the first electrode and the second electrode (fig. 2);

the second chip (LSI chip; noted: Suyama does not show separate chips as firs and second. However, Suyama does show all four LSI chips with identical structures as shown in figures 1 – 3) comprising:

a plurality of third electrodes 56 (with terminal 2a) which are arranged such that, when the first and second chips are combined together, the plurality of third electrodes contact the respective second electrodes of the first chip to interconnect the respective conductive lines of the chip (Noted: figure 2 illustrates: the first electrode 56 (of first chip) and the second electrode 57 (first chip) being contacted via terminal 2b and 2c; the third electrode 56 (of second chip) and the electrode 57 (second chip) being contacted via terminal 2b and 2c. The first electrode of the first chip and the third electrode of the second chip are connected with second electrode 57, therefore, third electrode will contact the common second electrode 57).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim **30** is rejected under 35 U.S.C. 103(a) as being unpatentable over Suyama (US Patent No. 6,403,463) in view of Shau (US Patent Application Publication No. 2002/0004932).

Regarding claim **30**, Suyama discloses the claimed invention of claim 19 but does not specify the LSI chips are a memory chip and a logic chip.

However, it is conventional and also taught by Shau that layout of a typical IC chip containing a core circuit block 101 (fig. 1) that is usually a combination of logic

circuit modules 102 (fig. 1) and memory modules 103 (fig.1). See [005] (starting at: Fig. 1).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the multi-chip module of Suyama with the typical IC chip modules of Shau, in order to achieve optimum use of silicon area for mass production ([0007], col. 2, lines 5 – 7).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Okamura (US Patent 5,619,472), Friedman et al (US 2002/0167829) and Ahn et al. (US Patent No. 6,441,479) disclose a system-on-a-chip with multi-layered metallized through-hole and semiconductor memory device similar to Suyama (US Patent No. 6,403,463) and Shau (US Patent Application Publication No. 2002/0004932).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Tran LT

October 27, 2004

David Nelms
Supervisory Patent Examiner
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